ABSTRACT OF THE DISCLOSURE

A method of partitioning an integrated circuit design for physical design verification includes steps of: (a) receiving as input a representation of an integrated circuit design having a number of physical design layers; (b) receiving as input a composite run deck specifying rule checks to be performed on the integrated circuit design; (c) partitioning the composite run deck into partitioned run decks so that the number of physical design layers referenced by each of the partitioned run decks is a minimum; (d) parsing the representation of the integrated circuit design to filter only the physical design layers required for each of the partitioned run decks into a filtered data deck for each of the partitioned run decks; and (e) generating as output the filtered data deck for each of the partitioned run decks.